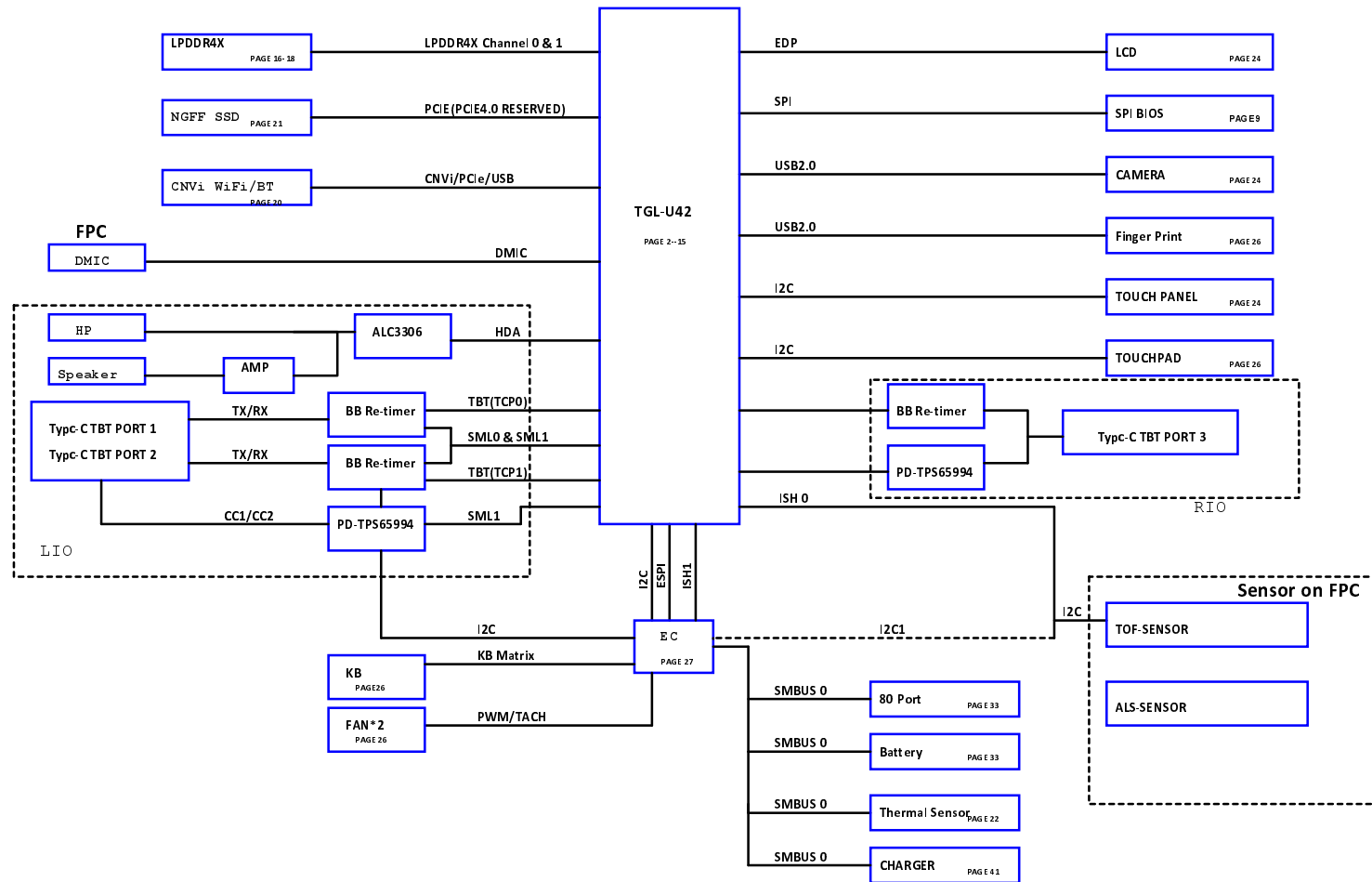
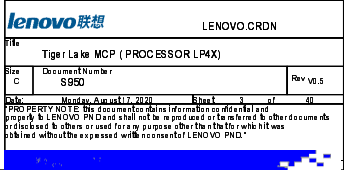


S950 TGL-U42 Schematic Block Diagram



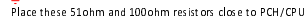
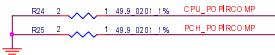


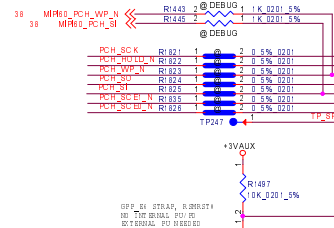
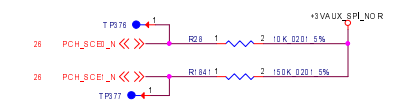
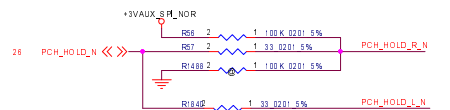
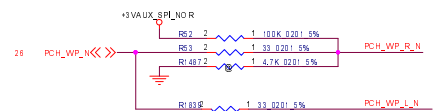
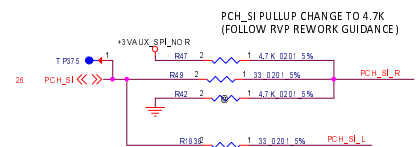
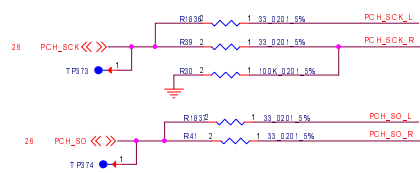
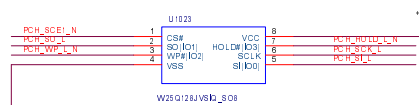
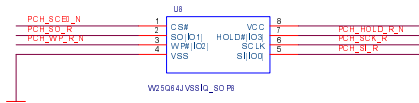
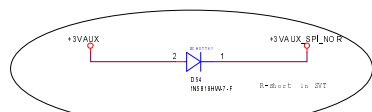
U51C

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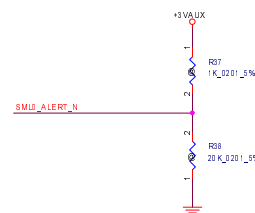
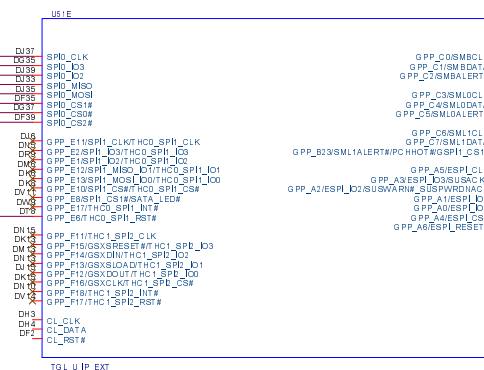




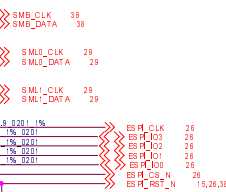
PCH_SI (SPI0_MOSI) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.

PCH_WP_N (SPI0_IO2) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.

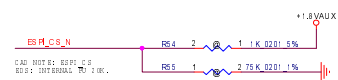
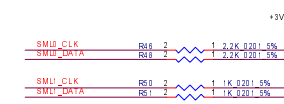
PCH_HOLD_N (SPI0_IO3) Strap, RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH.



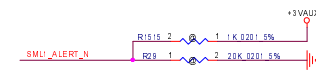
Boot Strap [0:3]=GPPC5,GPPH[0:2], RSMRST#
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI).
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.

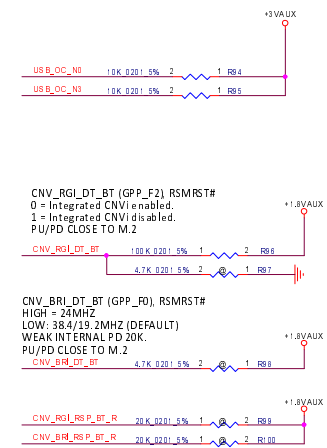
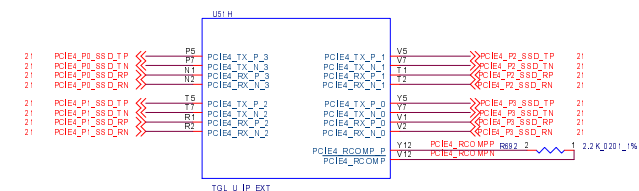


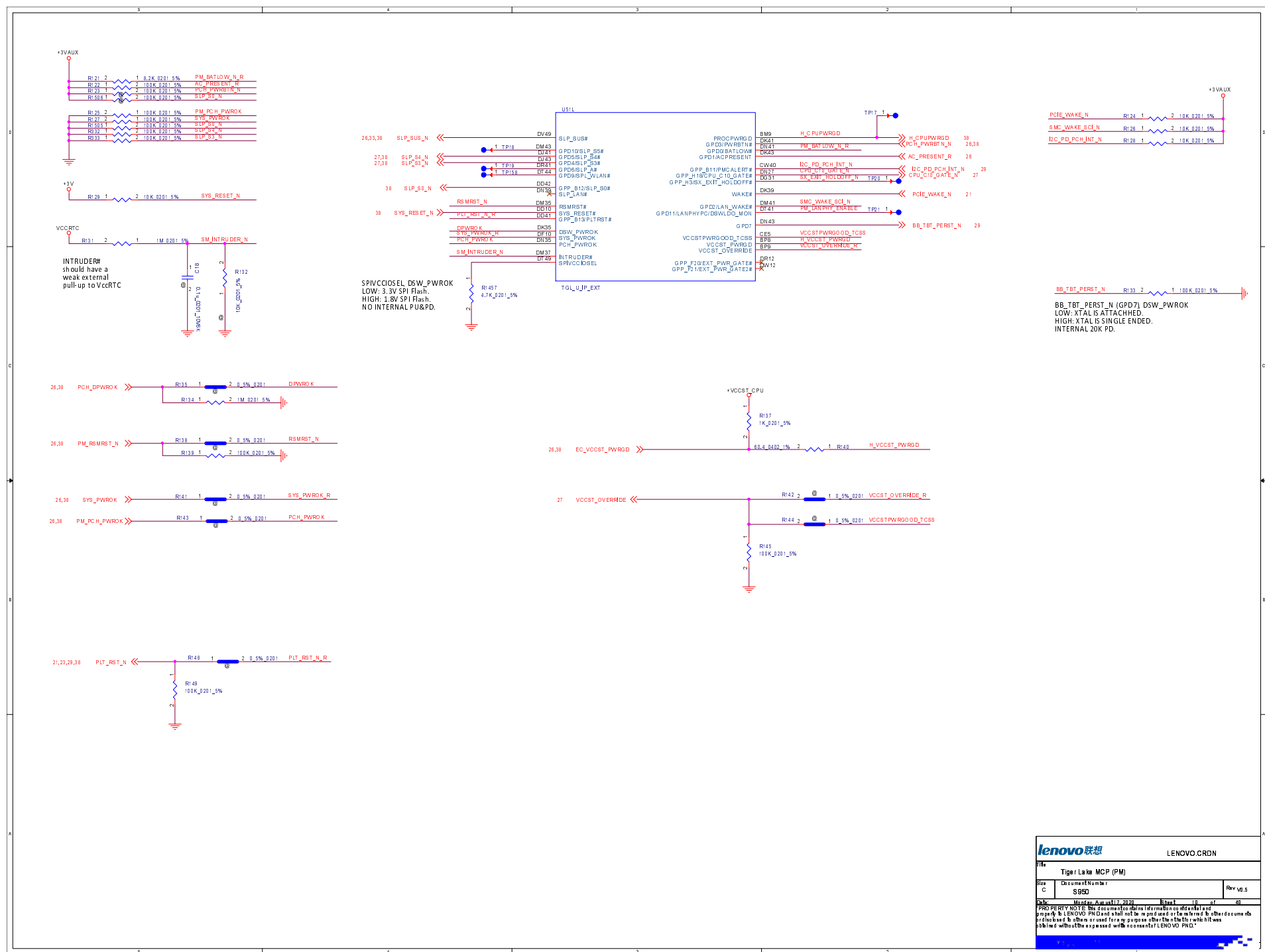
SMB_ALERT_N (GPP_C2) RSMRST#
This signal has a 20K-30% internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal pull-down is disabled after RSMRST# de-aserts.
2. This signal is in the primary well.



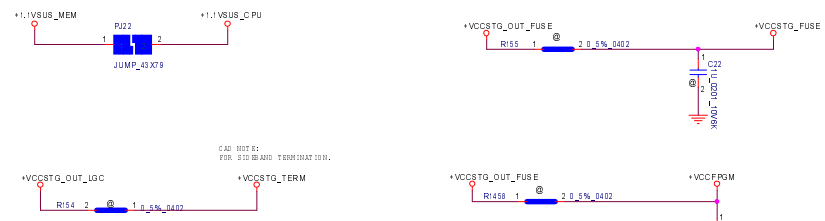
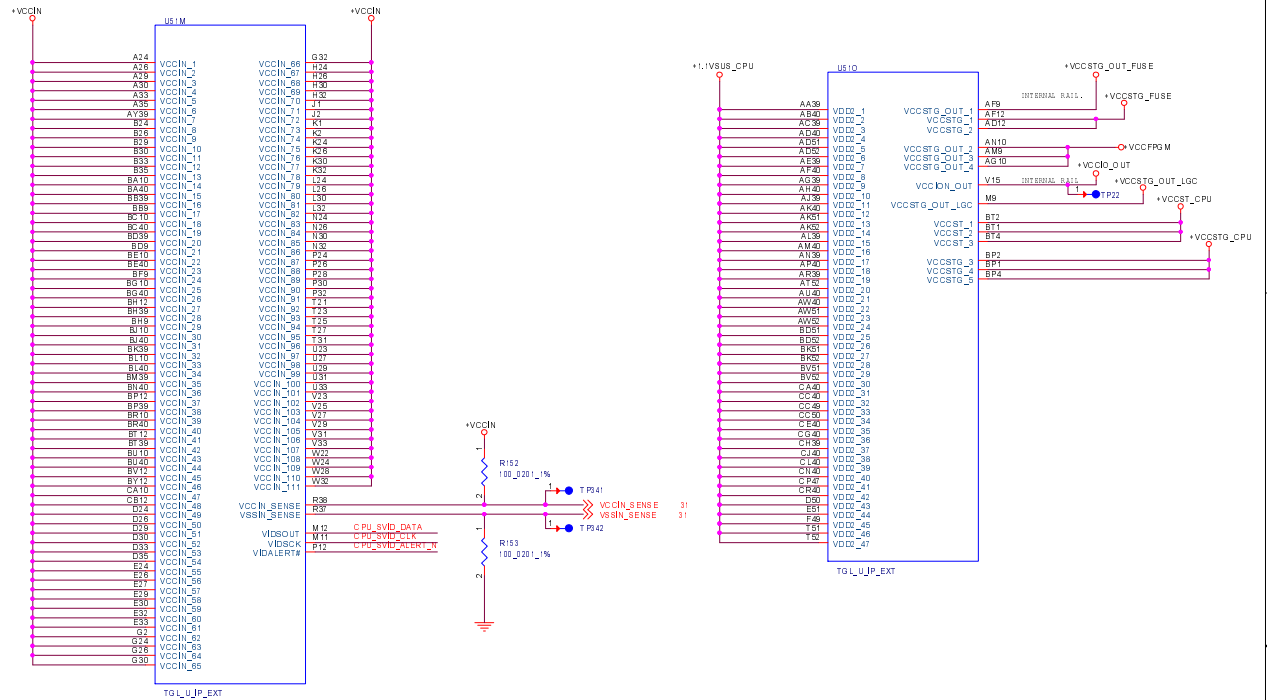
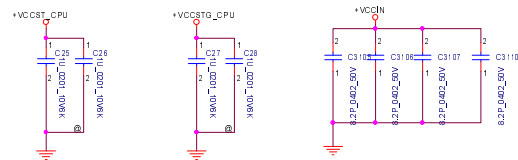
SMB_ALERT_N (GPP_B23) RSMRST#
0=38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
1=19.2MHZ CLOCK FROM DIVIDER
INTERNAL 20K PD.

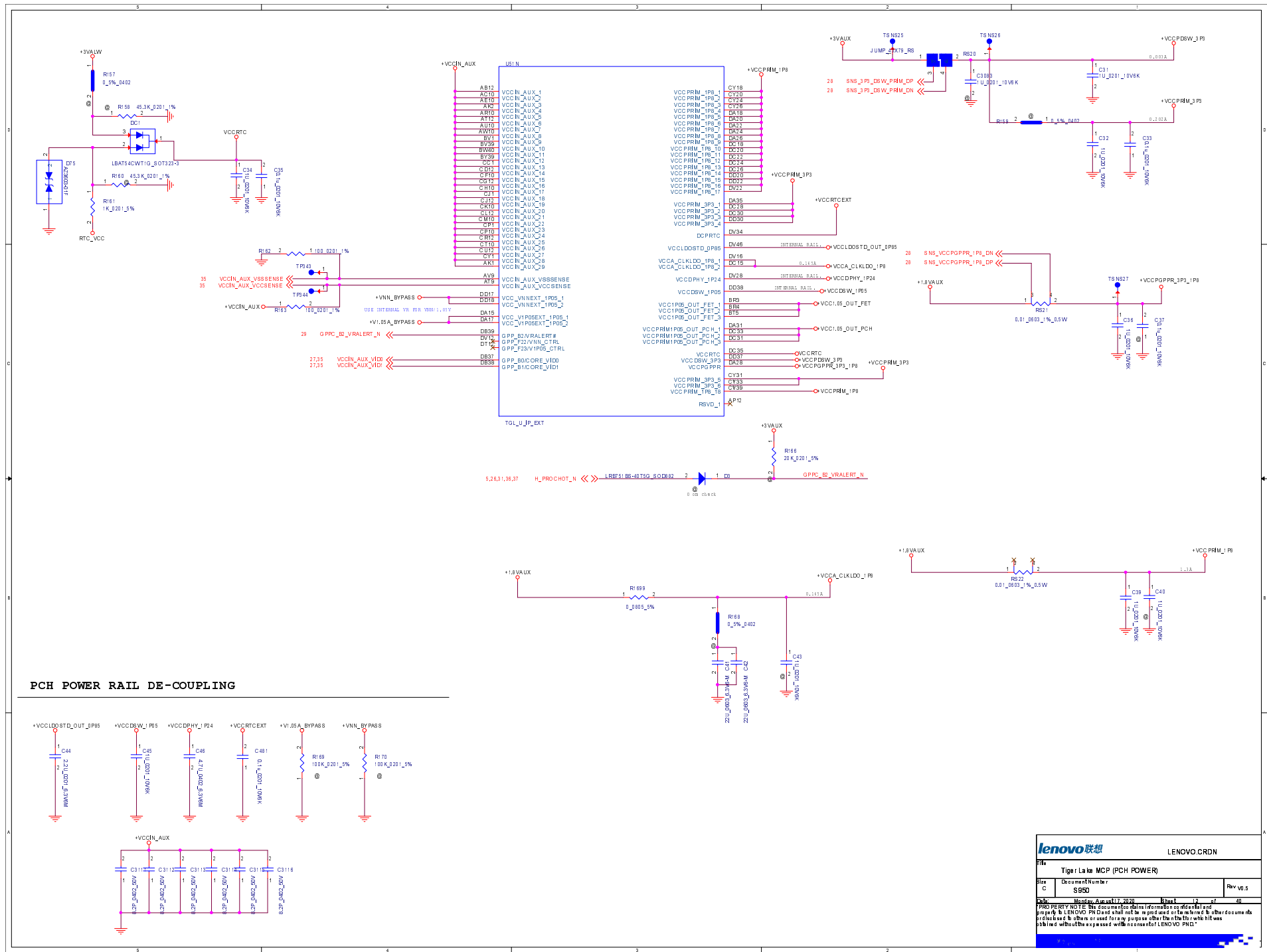


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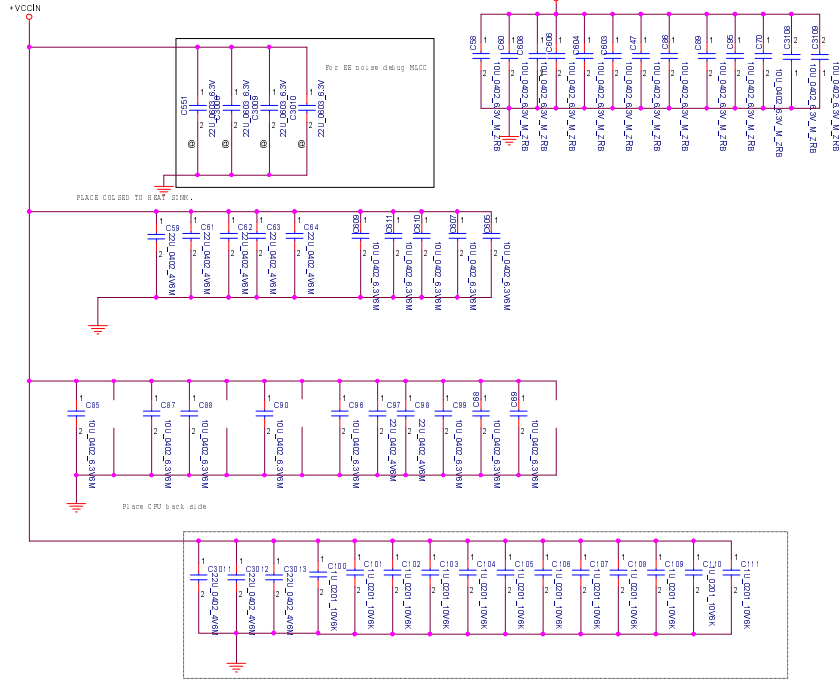


VCCST, VCCSTG VCCIN DE-COUPLING

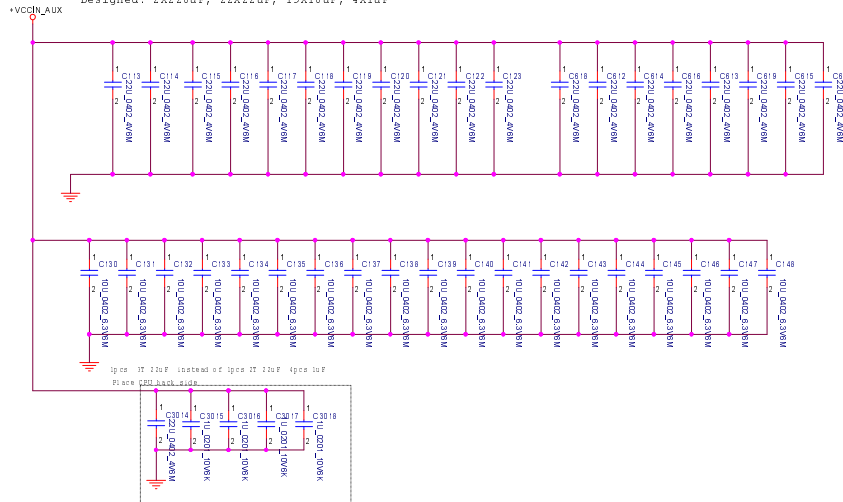




Required: 10X10uF, 20X10uF, 10X10uF, 10X10uF
Designed: 10X10uF, 20X10uF, 10X10uF, 10X10uF

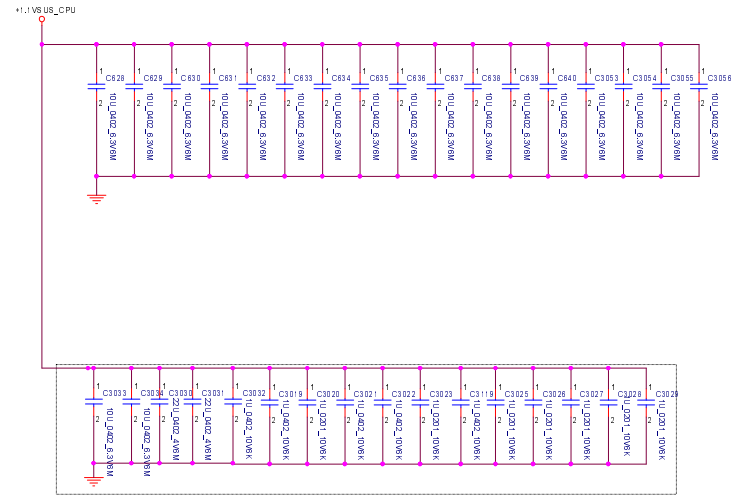


Required: 2X220uF, 6X47uF, 12X22uF, 17X10uF
Designed: 2X220uF, 22X22uF, 19X10uF, 4X1uF

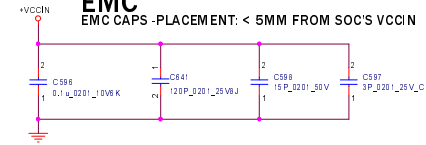


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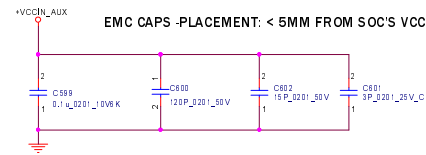
Required: 2X47uF, 10X1uF, 16X10uF
Designed: VR 6X22uF, 2X22uF, 14X1uF, 15X10uF



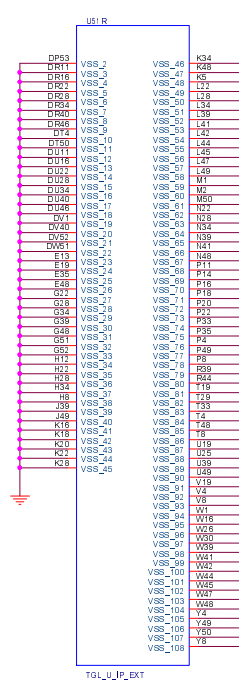
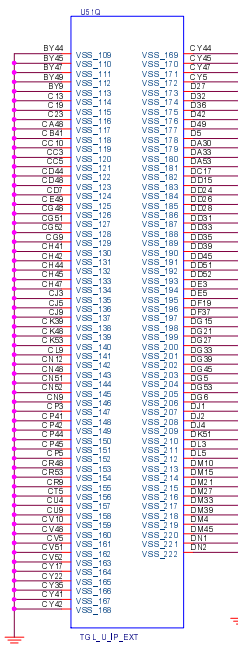
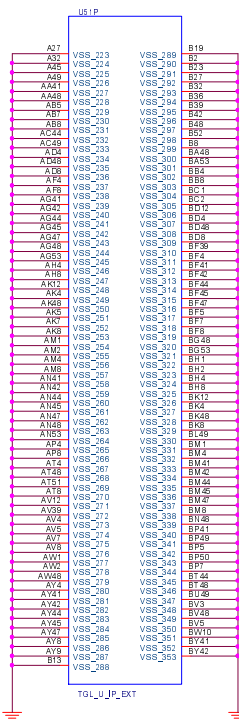
EMC
EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN



EMC
EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN_AUX



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File			
Tiger Lake MCP (Power CAP)			
Sheet	Document Number	Rev 0.0	
C	S950		
Date	Monday, August 17, 2020	Sheet	13 of 40
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LPDDR4X BGA 432 CHANNEL 0

The diagram illustrates the electrical connections for the LPDDR4X BGA 432 Channel 0. It features four channels (U24A, U24B, U24C, U24D) connected to a central BGA package (U24E). Each channel includes address, data, and control lines. Power and ground connections are shown for VDDQ_TX, VSSUS_MEM, and VSSUS_GND.

Channel U24A:

- Address: A0-A11
- Data: D0-D11
- Control: CS0, CS1, CKE0, CKE1, CLKA0, CLKB0, CLKA1, CLKB1

Channel U24B:

- Address: A0-A11
- Data: D0-D11
- Control: CS0, CS1, CKE0, CKE1, CLKA0, CLKB0, CLKA1, CLKB1

Channel U24C:

- Address: A0-A11
- Data: D0-D11
- Control: CS0, CS1, CKE0, CKE1, CLKA0, CLKB0, CLKA1, CLKB1

Channel U24D:

- Address: A0-A11
- Data: D0-D11
- Control: CS0, CS1, CKE0, CKE1, CLKA0, CLKB0, CLKA1, CLKB1

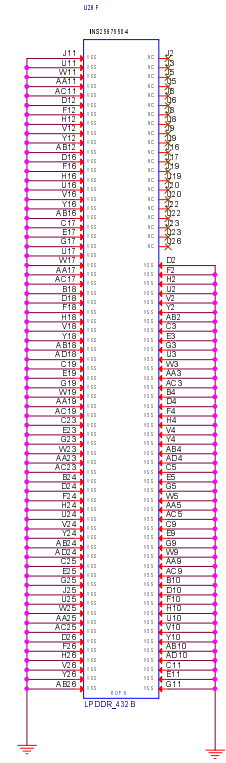
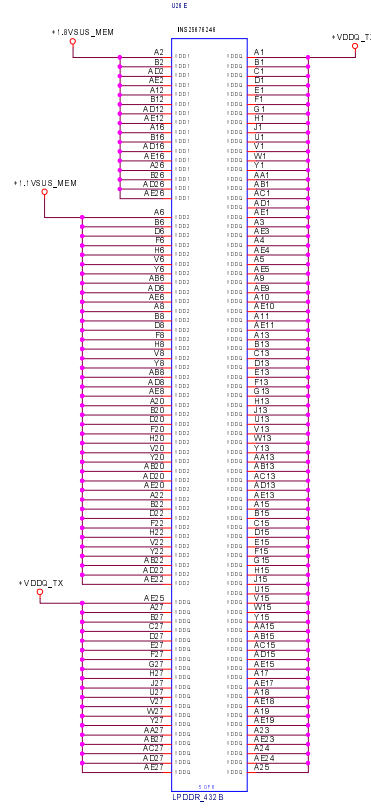
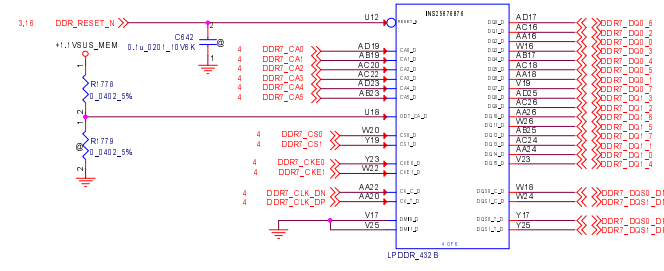
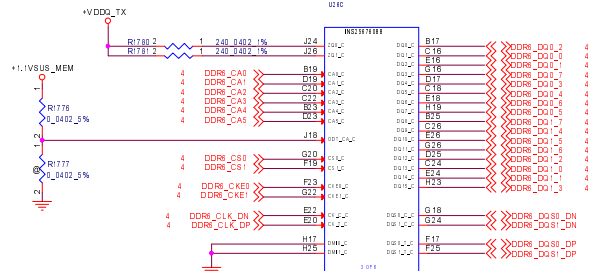
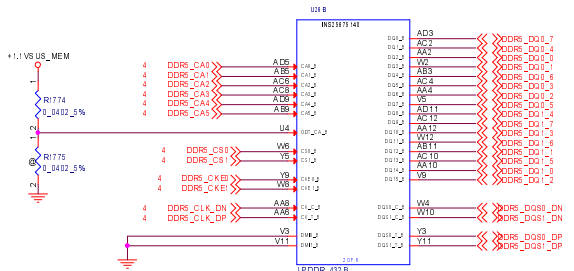
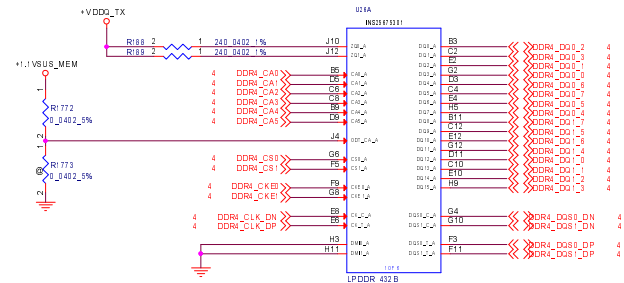
Power and Ground Connections:

- VDDQ_TX: Connected to the top of the BGA package.
- VSSUS_MEM: Connected to the bottom of the BGA package.
- VSSUS_GND: Connected to the bottom of the BGA package.

Legend:

- U24A: Channel 0
- U24B: Channel 1
- U24C: Channel 2
- U24D: Channel 3
- U24E: BGA 432

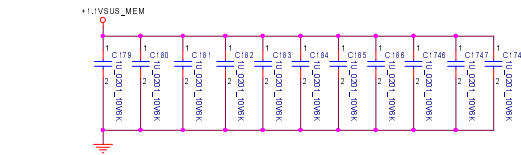
LPDDR4X BGA 432 CHANNEL 1



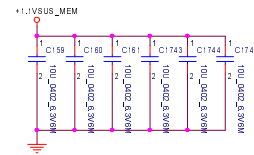
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LP4X-CH1 ON8D			
Size	Document Number	Rev	
C	S950	V0.5	
Date: Monday, August 17, 2020		Sheet	17 of 46
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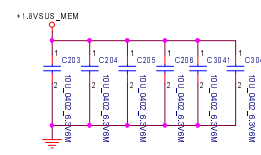
CAPACITORS FOR LPDDR4X CHANNEL 0



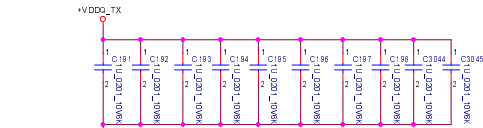
8 per dram, 2 per edge



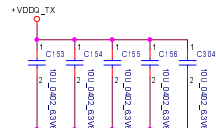
4 per Dram, 1 per edge



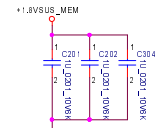
4 caps per dram, 2 per edge with the VDD1 BGAs



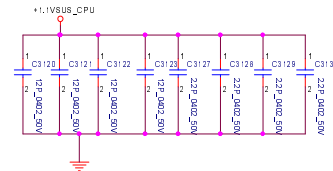
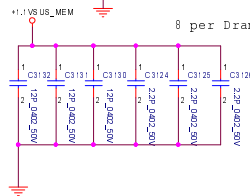
8 per Dram, 2 per edge



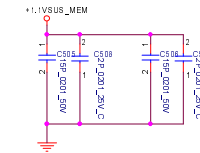
4 per Dram, 1 per edge



2 caps per Dram, 1 per edge with the VDD1 BGAs

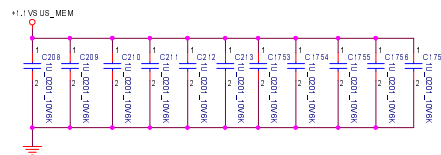


EMC CAP CHANNEL 0 AND 1

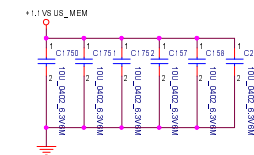


- EMC CAP:
1. PLACE 4MM FROM DRAM
2. PLACE EACH SET WITHIN 12MM

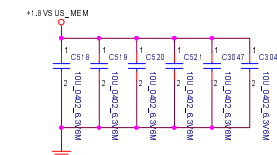
CAPACITORS FOR LPDDR4X CHANNEL 1



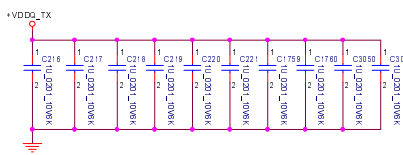
8 per dram, 2 per edge



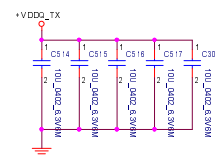
4 per Dram, 1 per edge



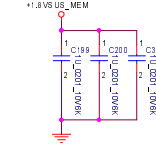
4 caps per dram, 2 per edge with the VDD1 BGAs



8 per Dram, 2 per edge



4 per Dram, 1 per edge



2 caps per Dram, 1 per edge with the VDD1 BGAs

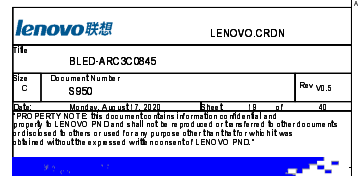
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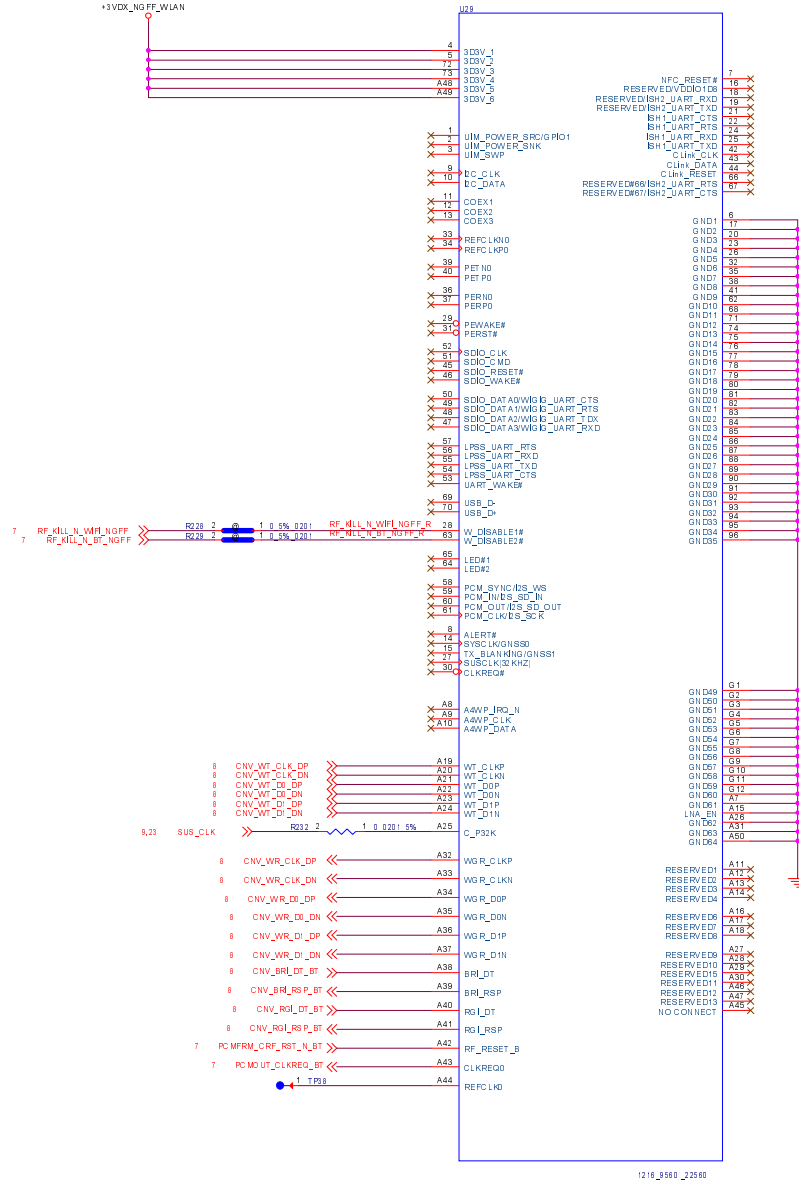
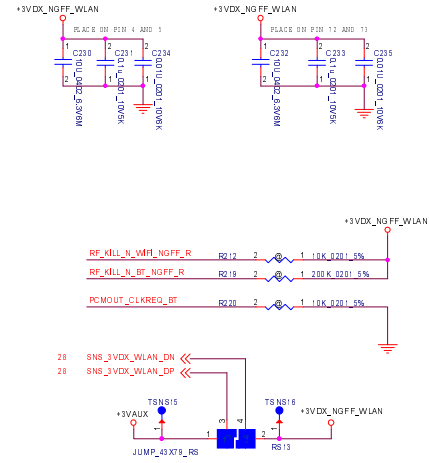
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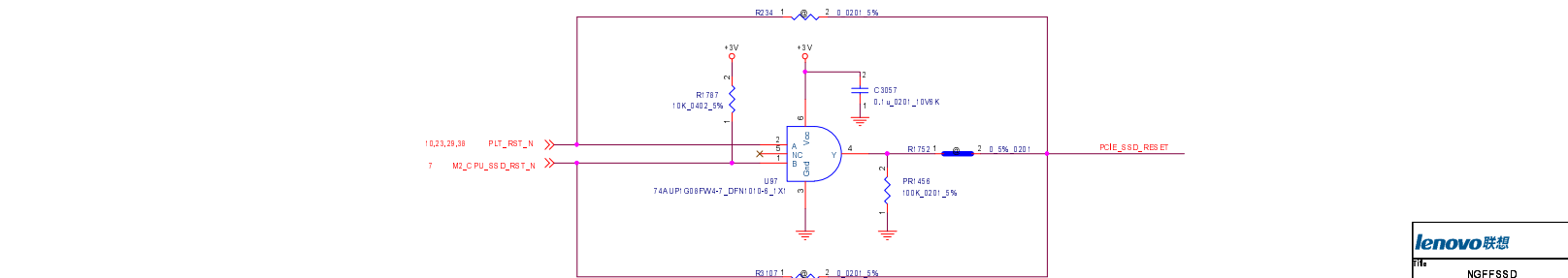
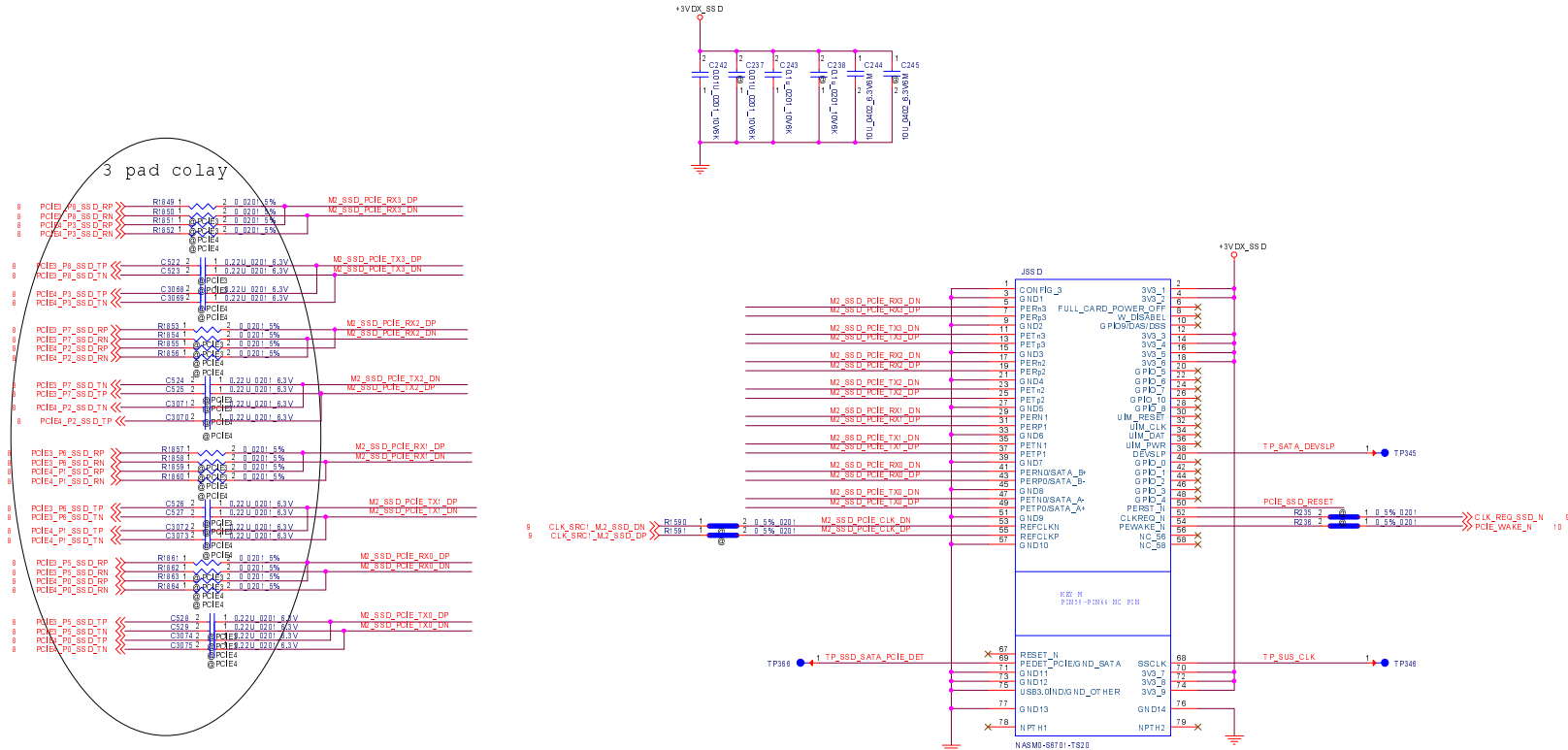
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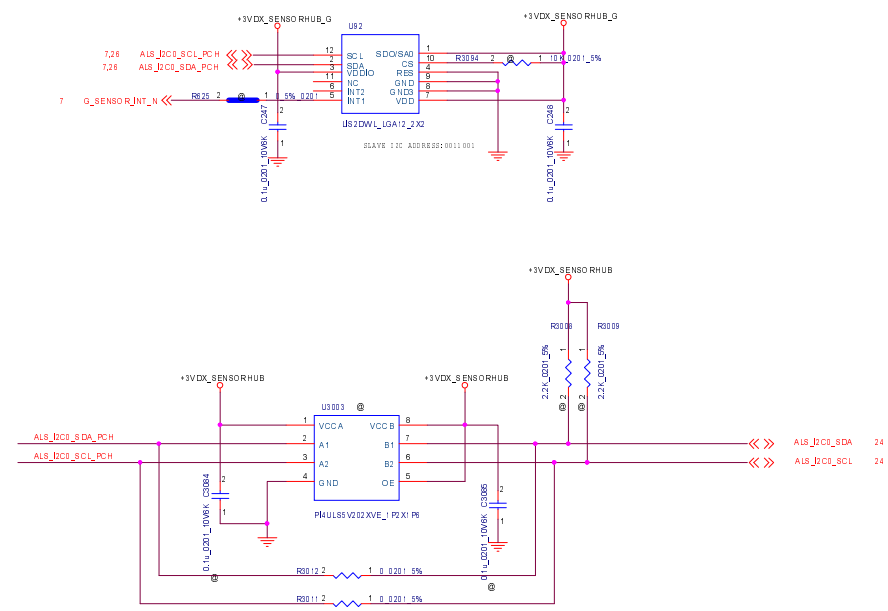
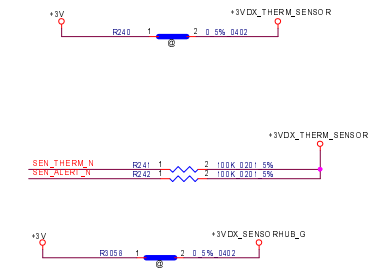
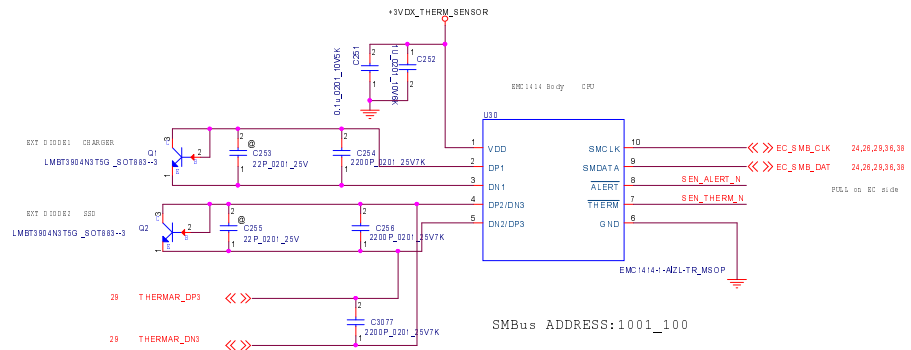


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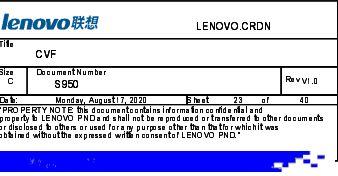
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C	S950		
Date: Monday, August 17, 2020 Sheet: 20 of 60			
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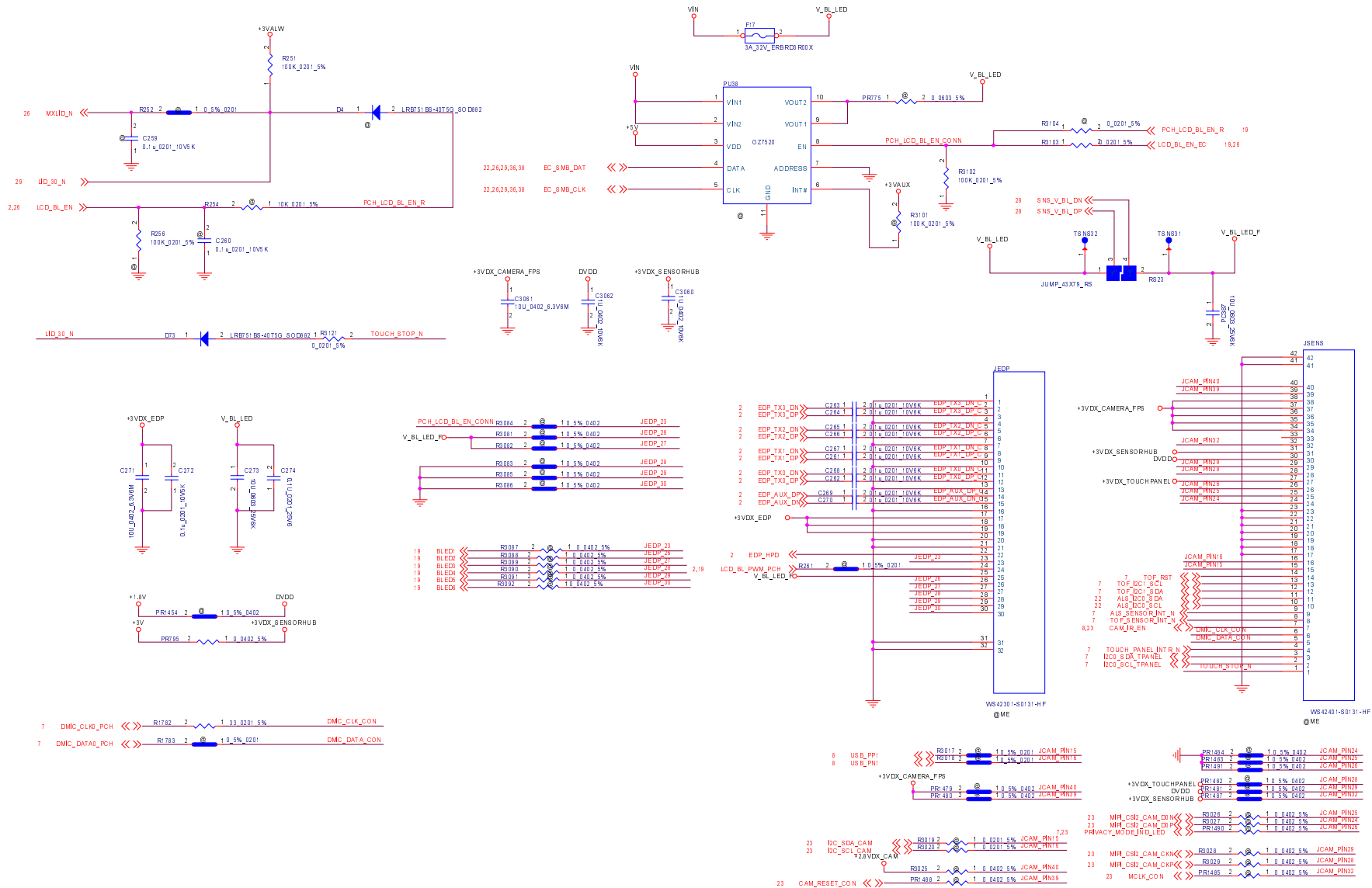
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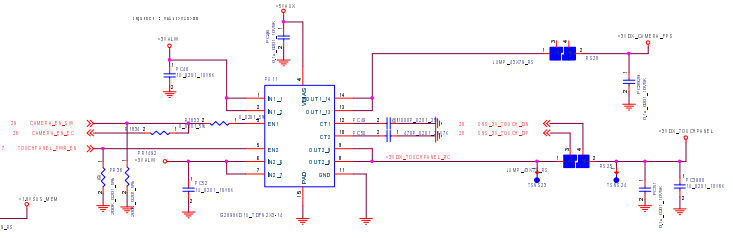
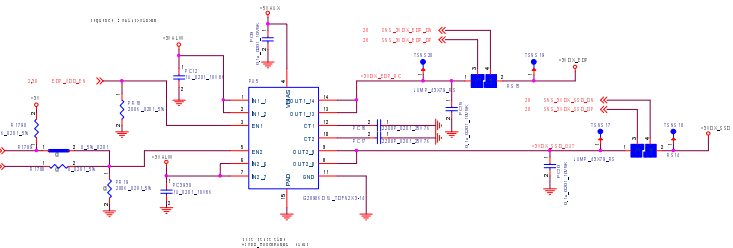
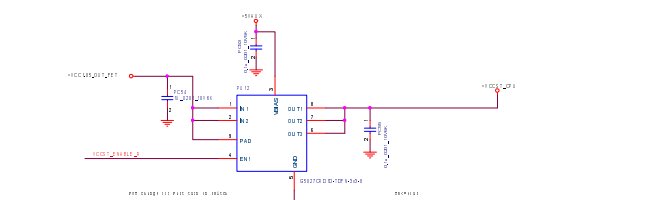


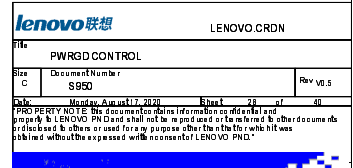


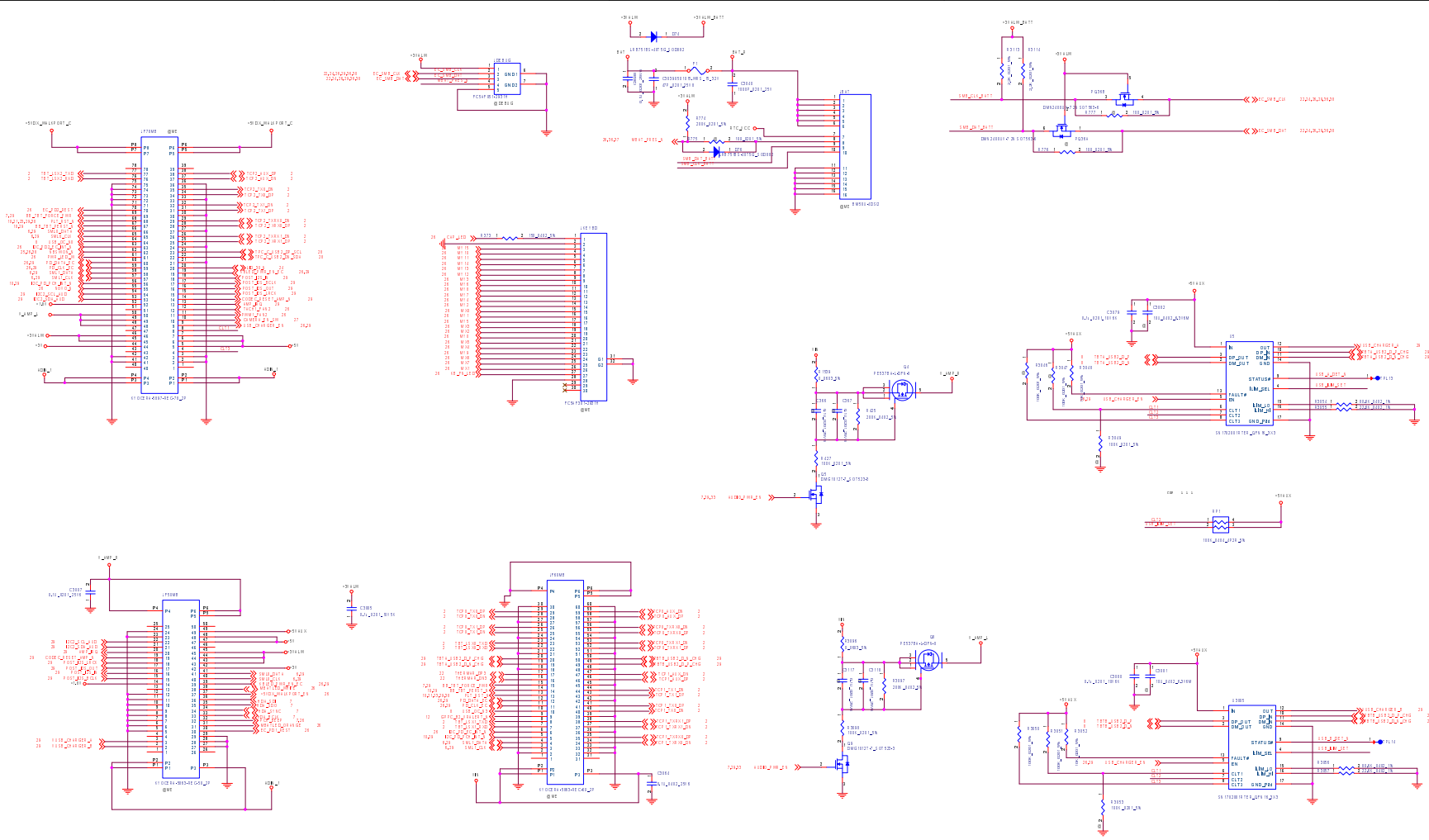
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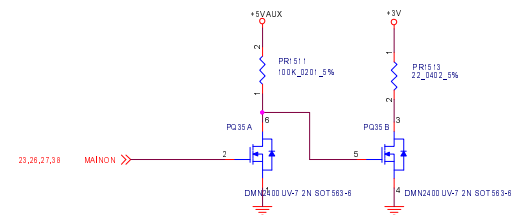
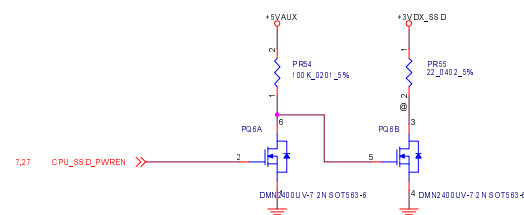
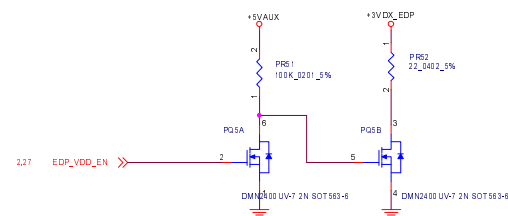
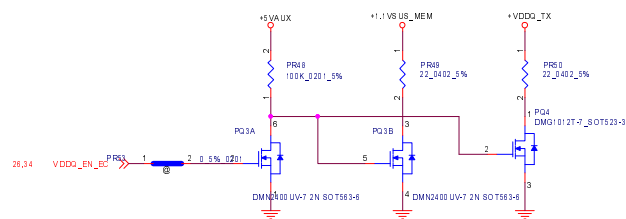


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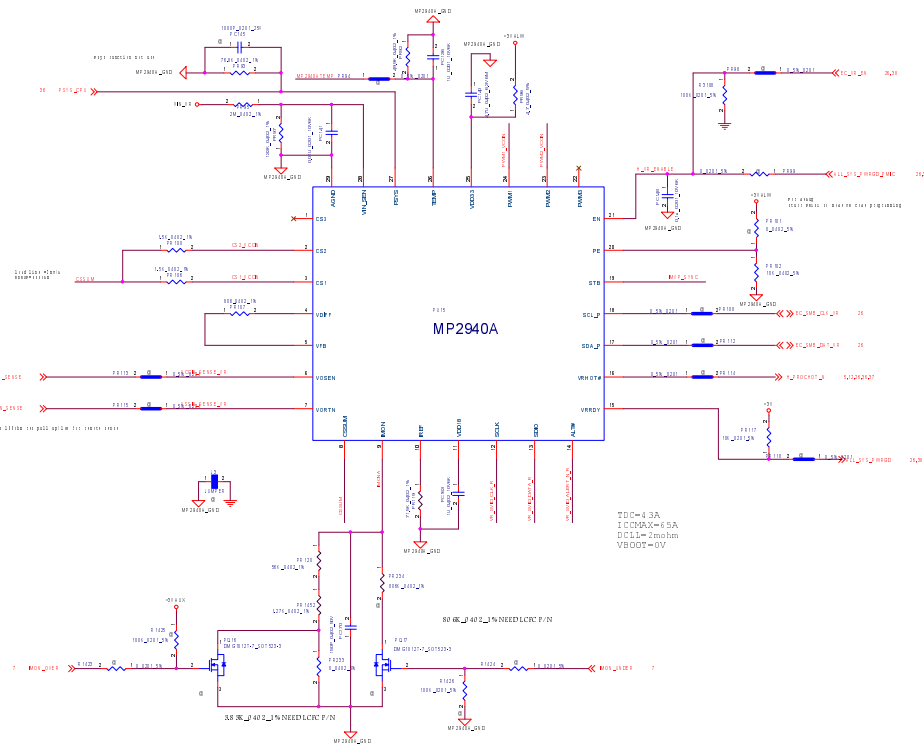




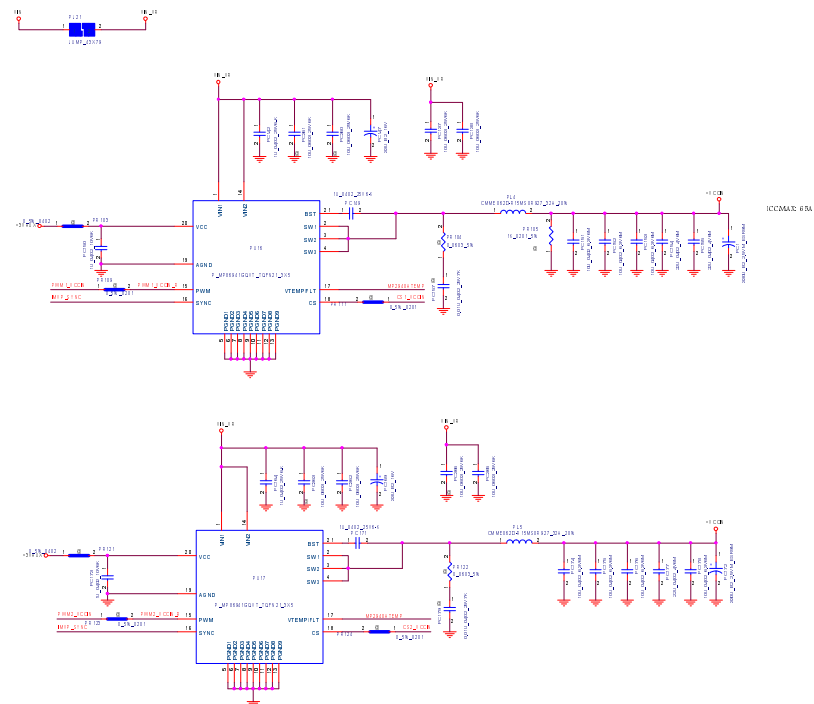
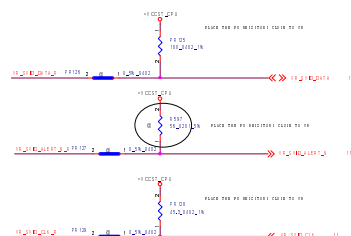
lenovo联想		LENOVO C500	
CONNECTOR			
Pin	Connector	Pin	Signal
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64
65	66	67	68
69	70	71	72
73	74	75	76
77	78	79	80
81	82	83	84
85	86	87	88
89	90	91	92
93	94	95	96
97	98	99	100



lenovo 联想		LENOVO.CRDN	
File			
DISCHARGE			
Size	Document Number		Rev
C	S950		0.5
Date: Monday, August 17, 2020 Sheet: 30 of 40			
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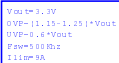


1. Normal (Default) : IMON_OVER = 1 and IMON_UNDER = 0
2. Performance Mode : IMON_OVER = 1 and IMON_UNDER = 1
3. Moderate Mode : IMON_OVER = 0 and IMON_UNDER = 0



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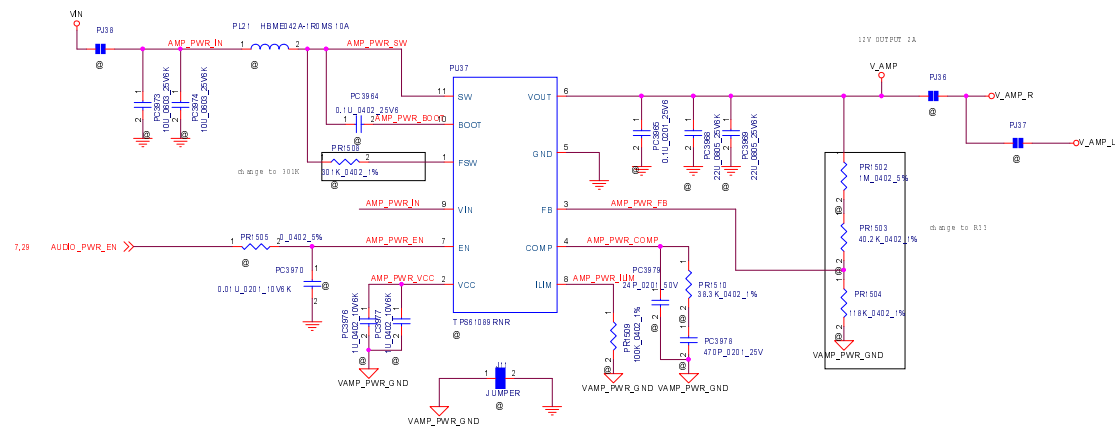
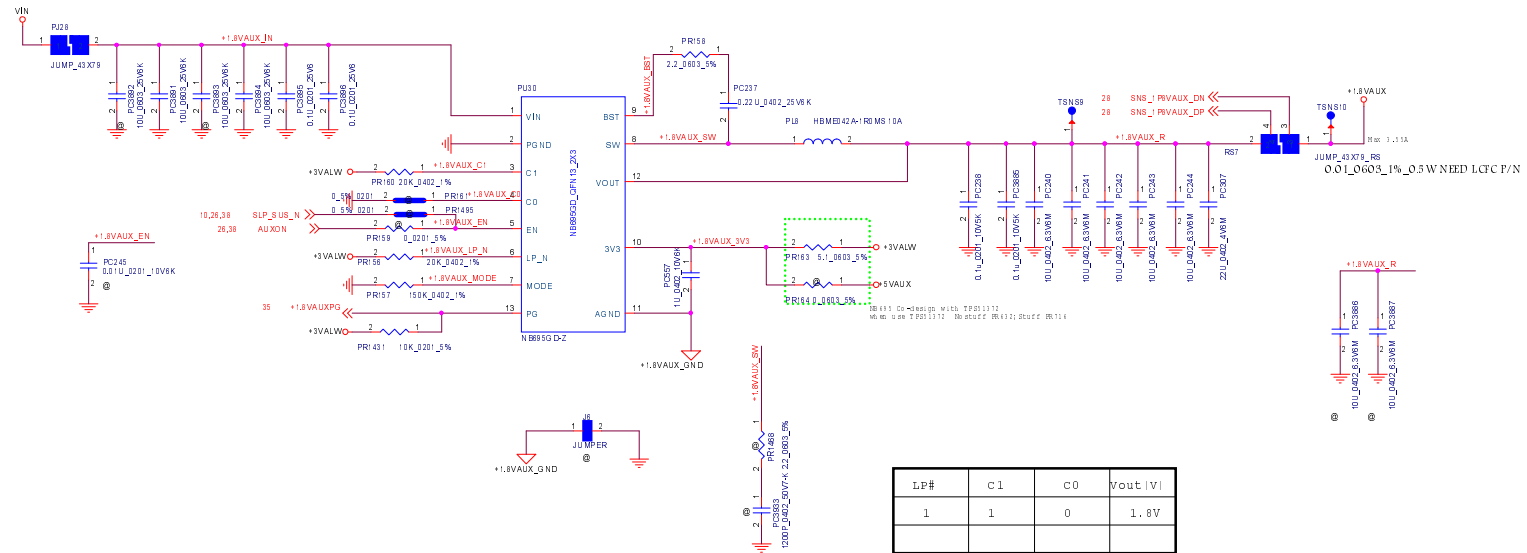
lenovo	
1	10V
2	10V
3	10V
4	10V
5	10V
6	10V
7	10V
8	10V
9	10V
10	10V
11	10V
12	10V
13	10V
14	10V
15	10V
16	10V
17	10V
18	10V
19	10V
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21	10V
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100	10V

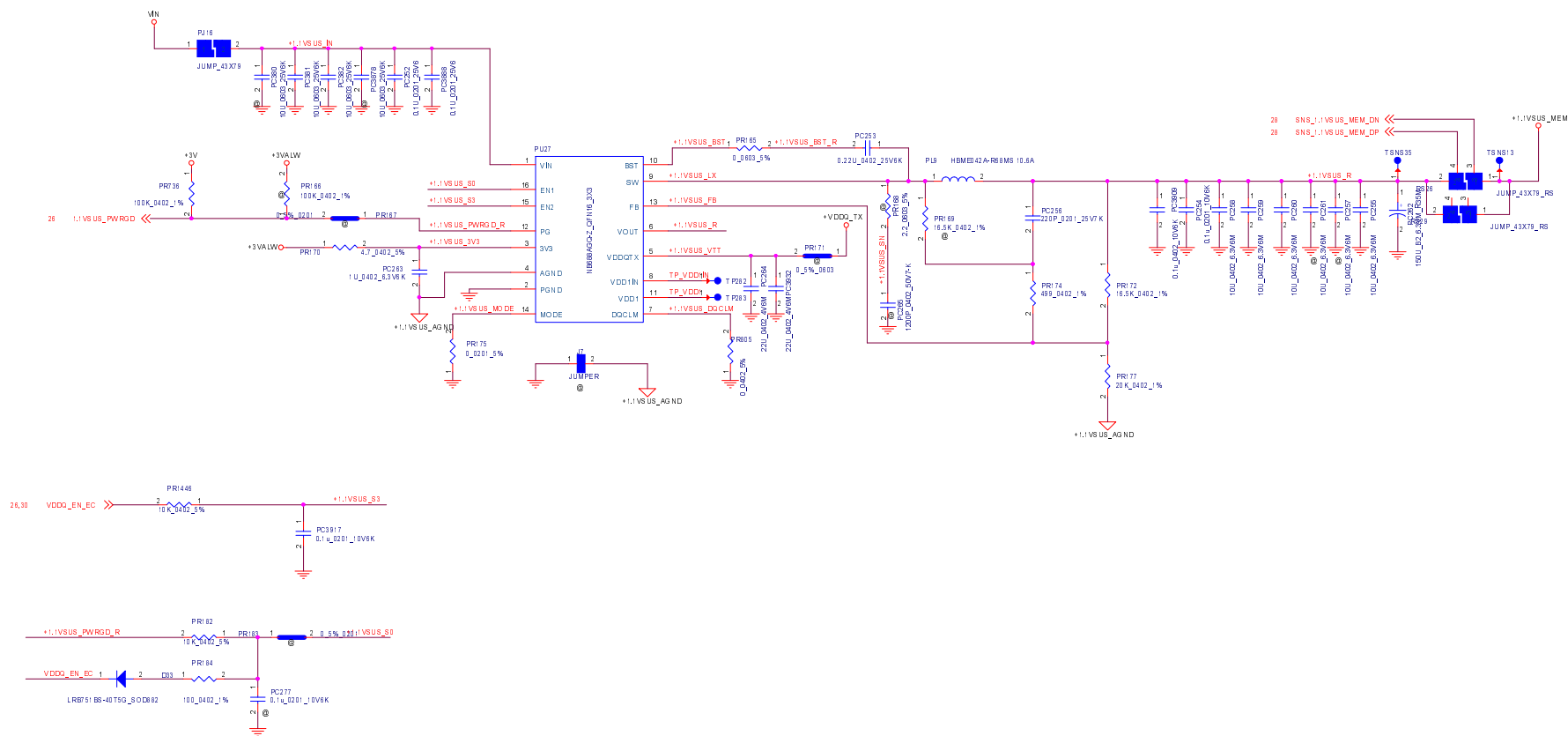


lenovo		联想		
		LENOVO C.R.W.		
A				
PW R_V_SVLAVI4V5WUX				
Item	Description Number			QTY
CPU	E 990			1
Memory	DDR3 4GB 1333MHz			4
Hard Drive	750GB SATA II 5400rpm			1
Optical Drive	DVD RW			1
Keyboard	US Keyboard			1
Mouse	Mouse			1
Power Supply	Power Supply			1
OS	Windows 7 Professional			1
Software	Microsoft Office 2010			1
Accessories	Lenovo Accessories			1
Total				

The above information is for reference only. The actual configuration may vary due to the change of the product specification or the availability of the components. Please refer to the latest configuration list for more details.

以上信息仅供参考。实际配置可能会因产品规格变更或组件可用性而有所不同。请参见最新的配置清单以获取详细信息。



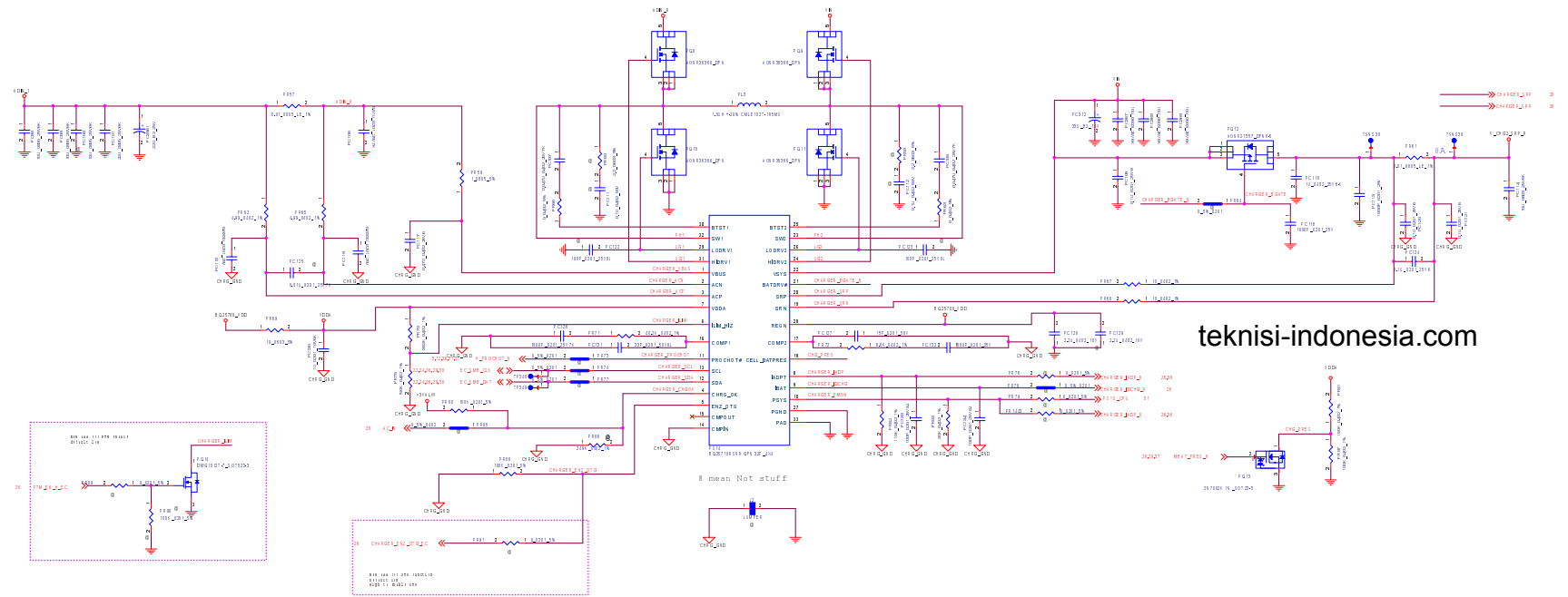


$V_{out} = 0.6 * (R1 + R2) / R2 = 1.215V$
 $OVP = (1.2 \sim 1.35) * V_{out}$
 $UVP = (0.7 \sim 0.8) * V_{out}$
 $R_{mode} = 0\Omega$ to set $F_{sw} = 700KHz$
 and select normal mode

STATE	EN1	EN2	+1.1VSUS	+1.8VSUS	+0.6V
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

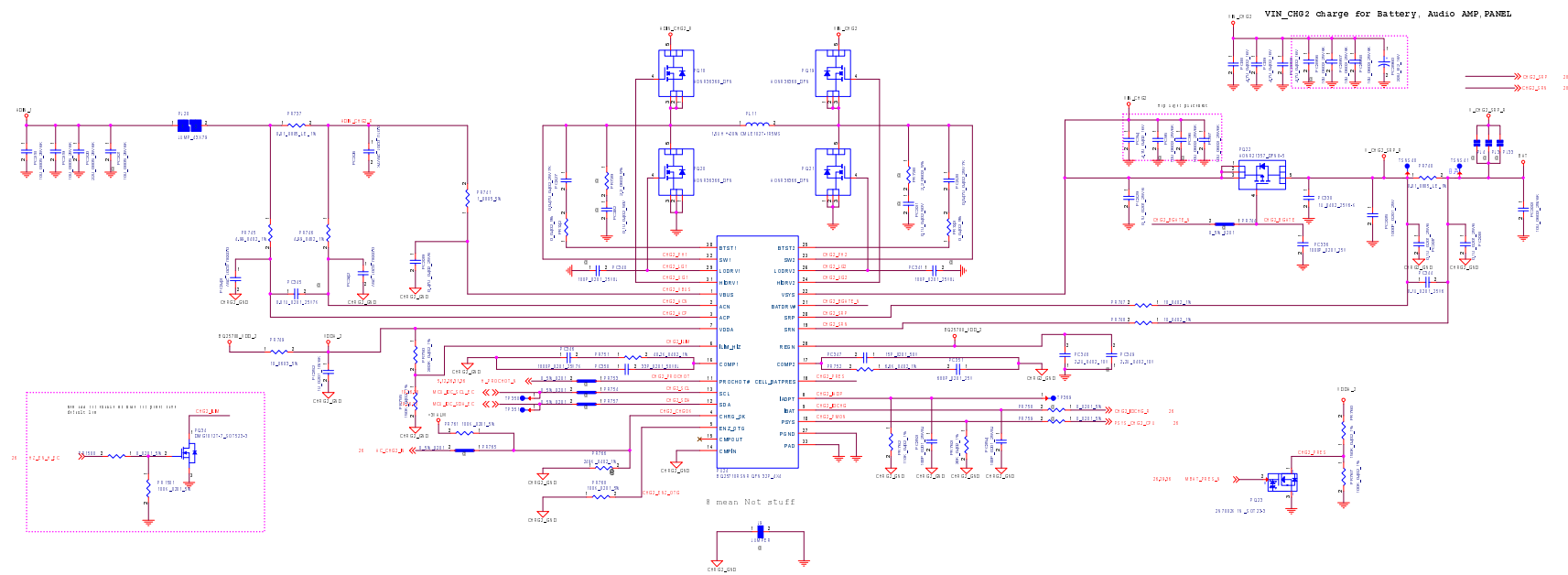
Note: S3 - sleep ; S5 - power off

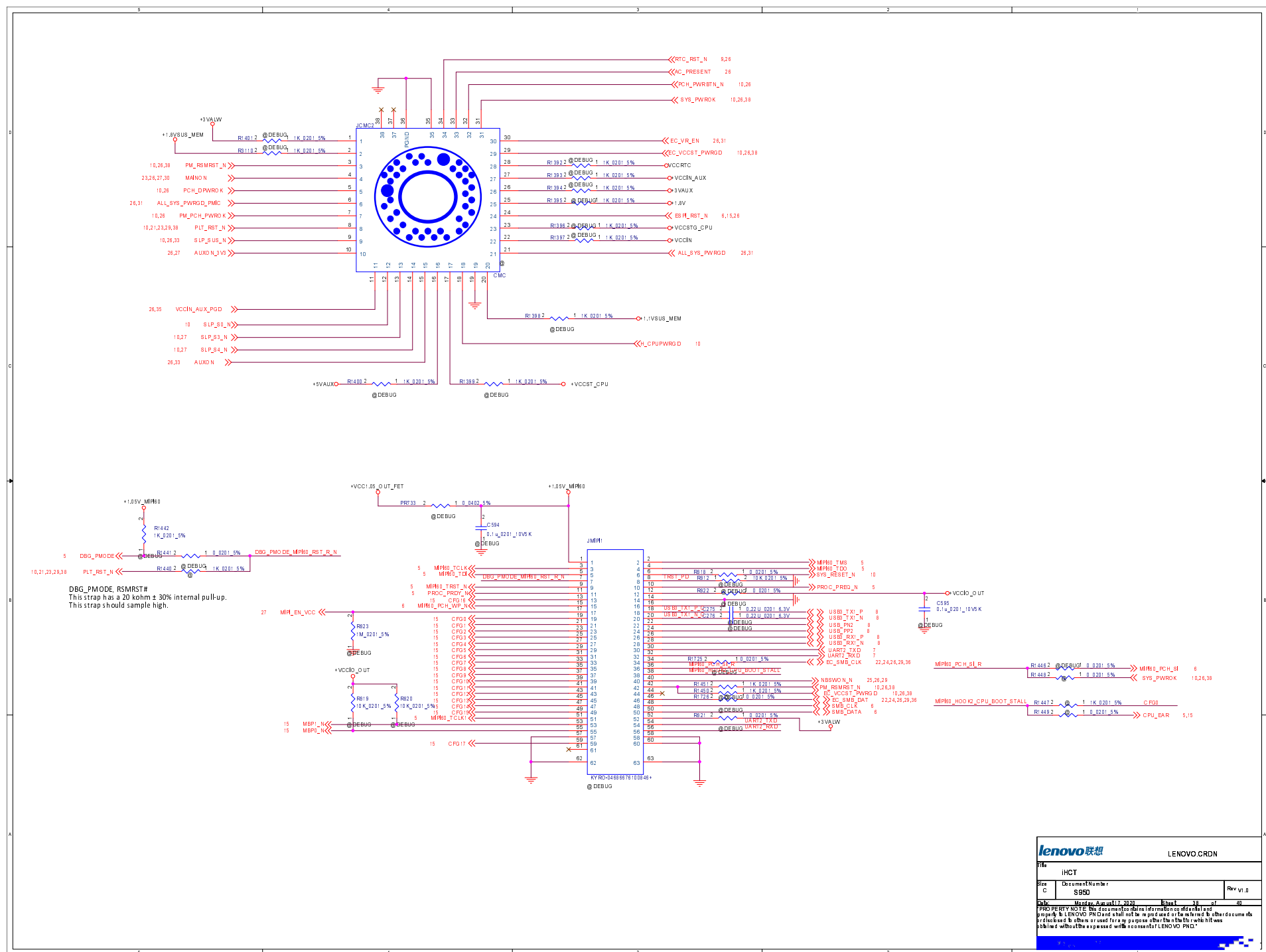
lenovo 联想
 LENOVO CRDN
 File: PWR_VDD1/VDDQ/VDDQ_MEM
 Size: S950
 Document Number: S950
 Rev: V0.5
 Date: Monday, August 13, 2018
 Sheet: 34 of 40
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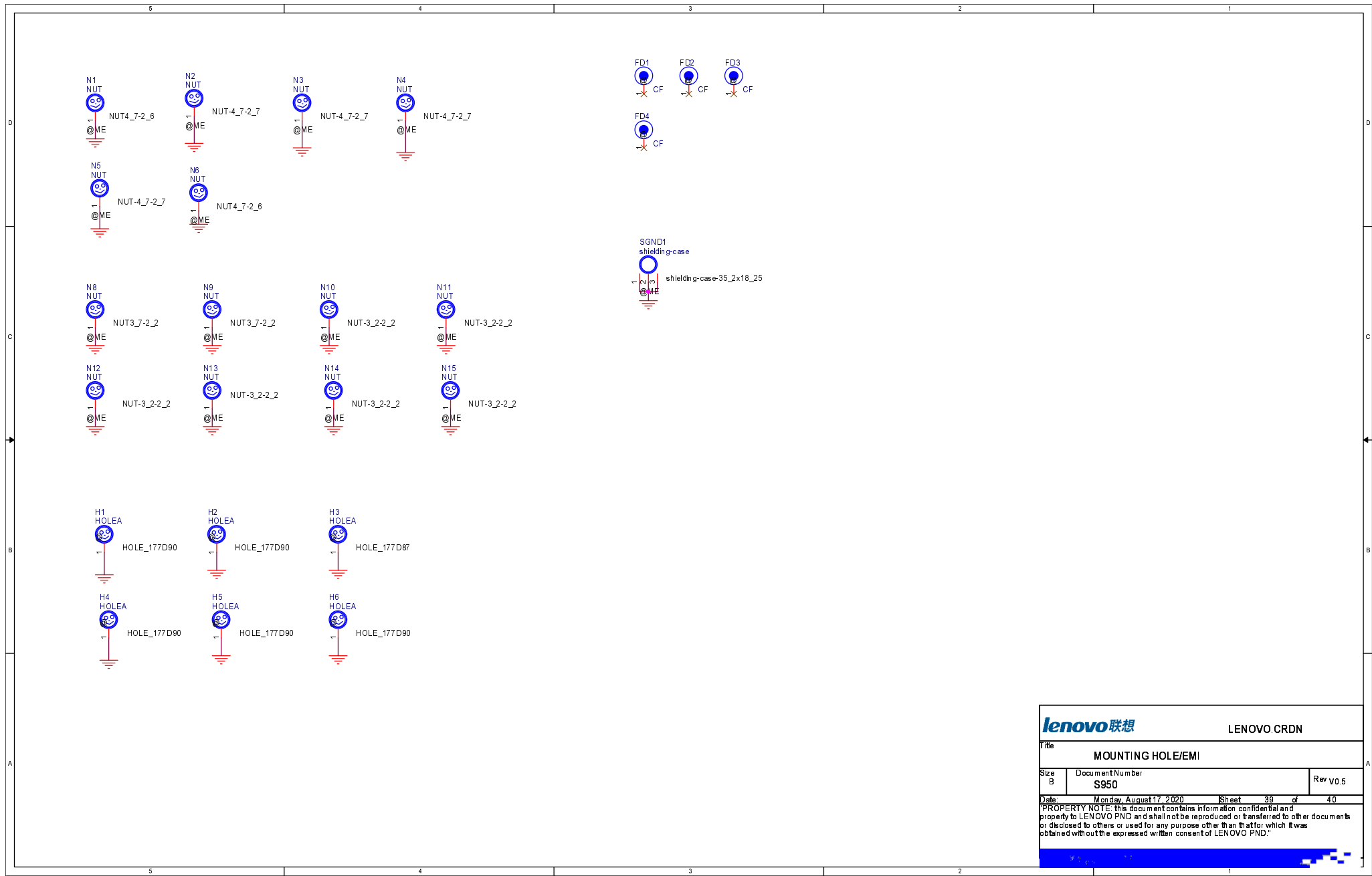


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NVC CHARGER			
REV	001	DATE	2018-01-11
DESIGNER	W. S. S. S.	DATE	2018-01-11
CHECKER	W. S. S. S.	DATE	2018-01-11
APPROVED	W. S. S. S.	DATE	2018-01-11
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Title			
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